(CS) chip select ⇒ A "low" on this input pin enables the communication between the 8255 and the CPU.

(RD) Read. ⇒ A "low" on this input pin enables 8255 to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to read from the 8255 PPI.

(WR) Write: A "Low" on this input pin enables the CPU to write data or control words into the 8255.

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch. Both pull up and pull down bus hold devices are present on port A.

Port B: One 8-bit data input/output latch /buffer and one 8-bit data input buffer.

Port C: one 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input) This port can be divided into two 4-bit ports under the mode control Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with port A and B.