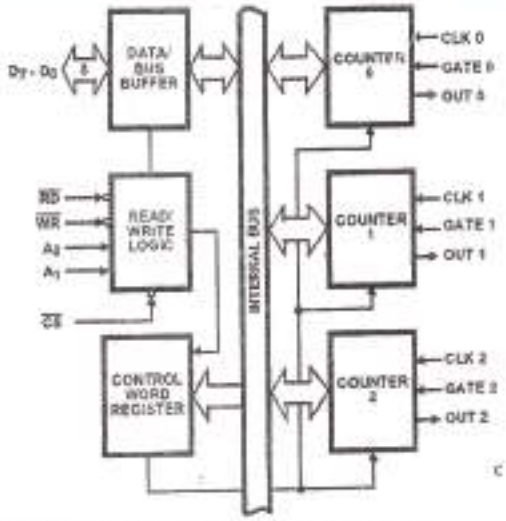
8254 PIT
(PROGRAMMABLE INTERVAL TIMER)

- IC **8254 is used** as a device to produce **Hardware delays**.
- It can **also be used** to generate a **real-time clock**, or as a **square wave** generator **etc.**
- Hardware delays are **more useful** than software delays because the µP is not actively involved in producing the delay. Thus when the delay is being produced the **µP is free** to execute its own program.
- The counting is done using **3 independent 16-bit down counters**.
- These counters can take the count in **BCD** or in **Binary**.
- After the Counter has finished counting and the required delay is produced, the 8254 interrupts the µP.

Architecture of 8254



The architecture of 8254 can be divided into the following parts:

1) Data Bus Buffer

- This buffer is used to **interface** the internal **data bus** with the external (system) data bus.
- It is thus connected to $D_7 - D_0$ form the µP.

2) Read Write Logic

- It accepts the **RD** & **WR** signals, which are used to **control** the flow of **data** through data bus.
- It also accepts the $A_1 - A_0$ address lines which are used to **select** one of the **Counters** or the **Control Word** as shown below:

A_1 A_0	Selection
0 0	Counter 0
0 1	Counter 1
1 0	Counter 2
1 1	Control Word

- It also accepts the **CS** signal to **select** the **8254** chip.

3) Control Word Register

SC_1	SC_0	RW_1	RW_0	M_2	M_1	M_0	BCD

SC_1 SC_0	Selection
0 0	Select Counter 0
0 1	Select Counter 1
1 0	Select Counter 2
1 1	**READ BACK COMMAND** (Only for 8254; Illegal for 8253)

RW_1 RW_0	Selection
0 0	**COUNTER LATCH COMMAND**
0 1	Read/Write LSB Only
1 0	Read/Write MSB Only
1 1	Read/Write LSB First and then MSB

M_2 M_1 M_0	Mode Selection
0 0 0	Mode 0 --- Interrupt On Terminal Count
0 0 1	Mode 1 --- Monostable Multivibrator
X 1 0	Mode 2 --- Rate Generator
X 1 1	Mode 3 --- Square Wave Generator
1 0 0	Mode 4 --- Software Triggered Strobe
1 0 1	Mode 5 --- Hardware Triggered Strobe

BCD	Type of Count
0	Binary Counter (1 digit → 0H ... FH)
1	BCD Counter (1 digit → 0 ...9)

- The Control Word Register is an **8-bit** register that holds the Control Word as shown above.
- It is selected when $A_1 - A_0$ contain 11.
- It has a different format when a Read Back command is given for **8254**, as shown below

Read Operations

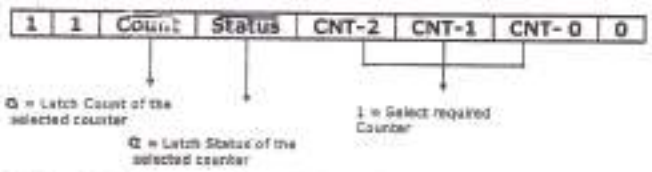
There are 3 ways in which the µP can read the current count:

A) **Ordinary Read**
- In this method, the **counting** is **stopped** by controlling the gate input of a selected counter.
- The Counter is then selected by $A_1 - A_0$ and IO Read operation is performed.
- First **IO Read** will give the Lower byte of the Count value, and the second IO Read will give the higher byte.
- The **disadvantage** here is that **counting** is **disturbed/stopped**.

B) **Read on Fly**
- In this method, the µP reads the **count** value **while** the **counting** is still in progress.
- Thus, it is called as **Read On Fly**.
- The appropriate value is written in the control word, and IO Read operation is performed.
- The current value of the **Count** is **"latched" internally** and returned to the µP.
- The **advantage** here is that counting is **not disturbed**.

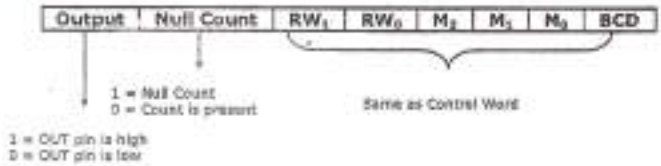
c) **Read Back Command**

Control Word Register for Read Back Command



- The Read Back Command is available **only** for **8254** and not for 8253.
- The Read Back Command **reads** the **Count** value in the **same manner** as **Read On Fly**.
- In **addition** to the Count, the current **Status** can **also** be **latched** using the Read Back command.
- Thus, the appropriate value (for latching the Count and/or Status of the selected counter) is placed in the Control word as shown above.
- The **advantage** here is that the **Count** and the **Status both** can be read **without disturbing the counting**.

Status Word (Status returned after the Read Back Command)



4) 3 Independent Counters

- 8254 has **3 Independent, 16-bit down counters**.
- Each counter can operate have a **Binary** or **BCD** count.
- Each counter can be in **one of** the **six** possible **modes**.
- Each counter can have a **max count** of 2^{16} = **65535 i.e. FFFFH**.
- Each counter has the following signals:

i. **Clk (Clock Input)**
ii. **Gate(Gate Input)**
iii. **Out (Clock Output)**

- The **input** clock signal is applied on the **CLK** line.
- The **counter decrements** the "**count value**" on **every pulse** of the **input clock at CLK**.
- **When** the **count** becomes **zero** (**Terminal Count i.e. TC**), the **status** of the **OUT** pin **changes.**
  This can be used to interrupt the µP.
- The **GATE** pin is used to **control** the **Counting.**
  In most modes, the **count** value gets **decremented only if** the **GATE** pin is **high.**